1. FEATURES

- Wide operating voltage range: 2.0V to 5.5V.
- 4-bit RISC type micro-controller with 75 instructions.
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Voice Duration (sec) @6KHz	ROM Size (10-bit)	I/O
85.0	208K x 10	16 (PA, PB, PC, PD)

  Program and voice data share the same ROM space.
- 336x4-bit RAM, divided into 6 pages.
- 2MHz instruction frequency.
- Slow mode to operate with low power consumption (+/- 3.0% accuracy).
- HALT mode to save power, less than 1uA@3V standby current.
- Built-in RC oscillation is accurate with +/- 0.5% frequency deviation.
- Low voltage reset (LVR=1.9V), watch-dog reset and I/O port reset are all supported to protect the system.
- Special hardware for LVR occurrence counting by program to manage low battery system operation.
- One interrupt entrance with an independent stack, multiple interrupt sources.
- 8-bit timer counter is applied to multiple clock source for various application.
- Low Voltage Detector (LVD) is built-in for monitoring the status of power and protect malfunction if unstable power is given.
- LDO regulator is supported for the power supply of SPI flash.
- Hardware SPI for external SPI devices data access. Dual power system operation supported (ex: VDD @ 5V, PB_VDD @ 3V).
- 16 flexible Bi-direction I/Os. Direction of each I/O is independently controlled by individual register bit.
- Each Bi-direction I/O pin can be optioned as different input and output function. For the input option, users can select one of three kinds of option: input with pull-high resistor, input without pull-high resistor, or input with register-controlled pull-high resistor (high-to-low wakeup only). For the output option, users can select one of three kinds of option: output with normal drive/sink sink current, large sink current or constant sink current.
- Shared pins to provide IR carrier, comparator, SPI interface and external reset feature.
- Infrared output: optional IR carrier frequency and optional data high/low IR output supported.

- Built-in voltage comparator for analog signal detection applications. Comparator output flag can be configured to generate interrupt and wakeup. Also, the flag can be used for timer counter clock source for specific application.
- Maximum of 6 channels can be played simultaneously, and each channel can be arbitrarily assigned as speech or MIDI channel.
- New high fidelity 4-bit / 5-bit mixed ADPCM or 10-bit PCM speech synthesis algorithm and ADSR with 256-step envelope for MIDI synthesis.
- Patented noise filtering algorithm with 250KHz over sampling to enhance signal-to-noise ratio and provide excellent sound quality without ROM size increase.
- 16-level digital volume control for synthetic speech/melody.
- Built-in hardware automatic Tone-Calibration of near-zero frequency deviation for precise tone frequency.
- High quality 12-bit D/A converter or 12-bit PWM driver.
- PWM driver can be normal PWM or Ultra PWM.

2. PAD DESCRIPTION

Pad Name	ATTR.	Description
VDD	Power	Positive power.
GND	Power	Negative power.
PA0/VIP	I/O	Bit 0 for Port A, or positive input of comparator.
PA1/VIN	I/O	Bit 1 for Port A, or negative input of comparator.
PA2/IR	I/O	Bit 2 for Port A, or IR carrier output.
PA3/Reset	I/O	Bit 3 for Port A, or external reset input.
PB_VDD	Power	Power for Port B and external component.
PB0/CSb	I/O	Bit 0 for Port B, or chip select pin for SPI interface.
PB1/SCK	I/O	Bit 1 for Port B, or serial clock pin for SPI interface.
PB2/SDO	I/O	Bit 2 for Port B, or serial data output pin (MOSI) for SPI interface.
PB3/SDI	I/O	Bit 3 for Port B, or serial data input pin (MISO) for SPI interface.
PC0~3	I/O	Bit 0~3 for Port C.
PD0~3	I/O	Bit 0~3 for Port D.
PWM1/DAC	O	PWM1 output or DAC output.
PWM2	O	PWM2 output.

3. CLOCK GENERATOR

The system clock is 2MHz, which is fast enough for many kinds of applications. The clock generator is a Ring oscillator, and users can only select the internal resistor oscillation (INT-R). The INT-R oscillator accuracy is up to ± 0.5%.

4. TIME BASE INTERRUPT

There are four kinds of time base interrupt period provided 0.256ms, 0.512ms, 1.024ms and 16.384ms.

5. IO PORTS

There are at most 16 I/O pins, designated as PAx through PDx, and x=0~3. All the I/O pins are bi-directional. An individual and independent register bit can determine the direction of each I/O pin.

Using as input pin of each I/O, there are 3 kinds of mask option. Users can select input with pull-high resistor, input without pull-high resistor, or input with register-controlled pull-high resistor (high-to-low wakeup only).

If users want to enable/disable pull-high resistor by register during program execution, only high-to-low level change on this pin can wakeup. On the other hand, if the pull-high resistor is fixed by option, either high-to-low or low-to-high level change on this pin can wakeup COB6.

The pull-high resistor of all the I/O pins has two kinds of option: weak and strong. The weak one is about 1.2MΩ@3V for normal application and the strong one is about 120KΩ@3V usually for key matrix function. When users decide this option, the same strength of pull-high resistor will be applied to every I/O pin.

Using as output pin of each I/O, there are 3 kinds of mask option. Users can select output with normal drive current and normal sink current, normal drive current and large sink current, or normal drive current and constant sink current.

The I/O pin PA2/IR is also a multi-function pin. PA2 can be optioned as IR carrier pin and IR carrier frequency can be determined by a 5-bit option. There is another option to determine IR carrier how is present according to data value is high or low.

The I/O pin PA3/Reset can be used as external reset pin by setting option. When PA3 is used as external reset, an active low signal on this pin will reset COB6.

6. SPI CONTROL INTERFACE

Port PB is assigned for SPI interface, PB0 to CSb, PB1 to SCK, PB2 to MOSI and PB3 to MISO. For the connection with external Flash, the applied pins are MOSI, MISO and SCK. The MISO is the input pin to receive data from the external device, and the MOSI is the output pin to deliver data. The SCK is the output pin to offer the clock signal, and configured as Option (8M/4M/2M/1M Hz). However, the CSb of enable pin for the external device can share with one of IO ports and define it as output.

SPI interface is built-in to communicate with external flash through Port PB. In order to keep the same voltage level as external devices, PB_VDD is designated for Port PB power, and it can be also the power for external SPI devices. There are two typical applications for PB_VDD connections. Case 1: PB_VDD is connected to VDD when PB_VDD status is set as floating. Case 2: PB_VDD is connected to external SPI VDD pin when PB_VDD status is set as internal LDO regulator (3.3V).

7. COMPARATOR

A voltage comparator is built-in for analog signal detection applications. Users can apply PA0 / PA1 to inputs of comparator by mask option. Basically, the output of comparator is represented for the level difference between VIP (PA0) and VIN (PA1). If output of comparator goes high, VIP is with higher level than VIN; low, VIP with smaller level than VIN. The comparator flag will be set to high while the level of VIP is bigger than VIN and won't be kept high even if the flag is clean and VIP is still bigger than VIN. Because the flag is controlled by a positive-edge clock source of register, the level of VIP has to be lower than VIP and the flag is clean by writing 0 to $INTF1. The flag will be launched while the level of VIP is bigger than VIN again.

8. LDO REGULATOR

A LDO regulator is built-in as the power of PB0~3 to support SPI applications. Users can set 3.3V and internal power from LDO regulator through register $SPIV for SPI interface. The LDO regulator supplies enough power consumption for reading data from SPI flash, but programming SPI flash won't be supported due to less supply current of LDO (10mA). Particularly, the LDO regulator is designated for SPI interface, not normal IO. If users apply to control high-consumption device, i.e. LED, the application won't work as expected. Please note that a 0.1uF capacitor nearby PB_VDD pin is necessary to stabilize the voltage if LDO regulator is enabled.

9. LOW VOLTAGE DETECTOR (LVD)

There is one hardware voltage detector in COB6. It offers four levels for various application, 2.4V, 2.7V, 3.6V and 4.1V controlled by register $LVD. The voltage detection function has to be enabled first, then select specific level for application, the flag will go to high while VDD is higher than selected level. User can check power status by setting different level and monitoring the flag. In general, for 2-battery application, 2.4V/2.7V will be chosen; 3-battery application, 3.6V/4.1V.

10. AUDIO SYNTHESIZER

COB6 provide 6-CH Speech/MIDI synthesizer to play voice and patch-wave melody. All synthesis is provided by hardware and each channel can synthesize voice/MIDI independently.

COB6 provide two kinds of Audio Output: one is 12-bit DAC and the other is 12-bit PWM direct-drive.

10.1 Voice

COB6 supports 10-bit PCM and encoded 4-bit / 5-bit mixed ADPCM speech data. The PCM voice quality is higher, but it occupies double ROM space than the ADPCM one. By cooperating with embedded noise filter of 250KHz over-sampling, it could decode high fidelity voice data even if you adopt ADPCM voice. It means you could store longer voice duration or provide more kinds of patch at lower sampling rate but enrich user's applications without degradation of sound quality.

10.2 Midi

COB6 provide three kinds of method to construct a patch-wave of timbre (instrument). The first method is to record a complete waveform, then play it by playing whole wave only. It is usually called "Head Only". This is the best way to represent a best quality melody at the expense of ROM space.

The second method is called "Head wave + Tail Loop" with envelope information representing ADSR (Attack-Decay-Sustain-Release). It is the recommended way to construct a patch-wave, which can provide high quality melody without sacrificing too much ROM space.

The third method is to use periodic portion of an instrument to represent a patch. It is called "Tail Loop". This method will occupy less ROM space with acceptable audio quality.

10.3 Audio Output

COB6 provide two kinds of audio output: one is 12-bit DAC and the other is 12-bit PWM direct-drive. By programming register CHARC[3] with appropriate value, users can select one of them to synthesize audio signal to drive external speaker.

When using the PWM output, we provide an option of normal PWM current or ultra PWM current for different customer demand. The ultra PWM consumes more current and makes sound louder.

10.4 Volume Control

There are 16 steps volume control, which can be applied to synthetic digital data for the Mixer output no matter DAC or PWM direct-drive is selected.

When users write value to register VOL[3:0], this value will multiply with Mixer output to adjust the volume of final synthetic result.

11. WATCH-DOG TIMER (WDT)

To recover from program malfunction, COB6 supports an embedded watch-dog timer reset. Users have to clear the WDT periodically to prevent from timing up with a reset generation.

Typically, the minimum time-up period of the WDT is about 28ms and users can clear WDT through instruction CWDT.

12. OPERATING MODE

COB6 provide 3 kinds of operating mode: Normal, Slow and Halt mode. After power is turned on, COB6 will start its reset process. The power on stable time is about 131ms. After reset process is completed, COB6 will enter Normal mode.

In Normal mode, the system clock is 2MHz. User can implement sorts of application in this mode. On the other hand, users can select Slow mode or Halt mode to save power consumption.

12.1 Slow Mode

COB6 will enter Slow mode if SLOW instruction is executed. The system clock of Slow mode is about 13.6 times slower than that of Normal mode, and the frequency accuracy is +/- 3.0%. The instruction will not be executed at Slow mode.

COB6 can wake up from Slow mode by interrupt request or level change on I/O pin. The stable time after wake up from Slow mode is about 50us.

12.2 Halt Mode

COB6 will enter Halt mode if the HALT instruction is executed. At Halt mode, system clock is completely disabled and all IC functions stop to minimize the power consumption.

The only way to wake up COB6 from Halt mode is level change on I/O pin. The stable time after wake up from Halt mode is about 50us.

13. ELECTRICAL CHARACTERISTICS

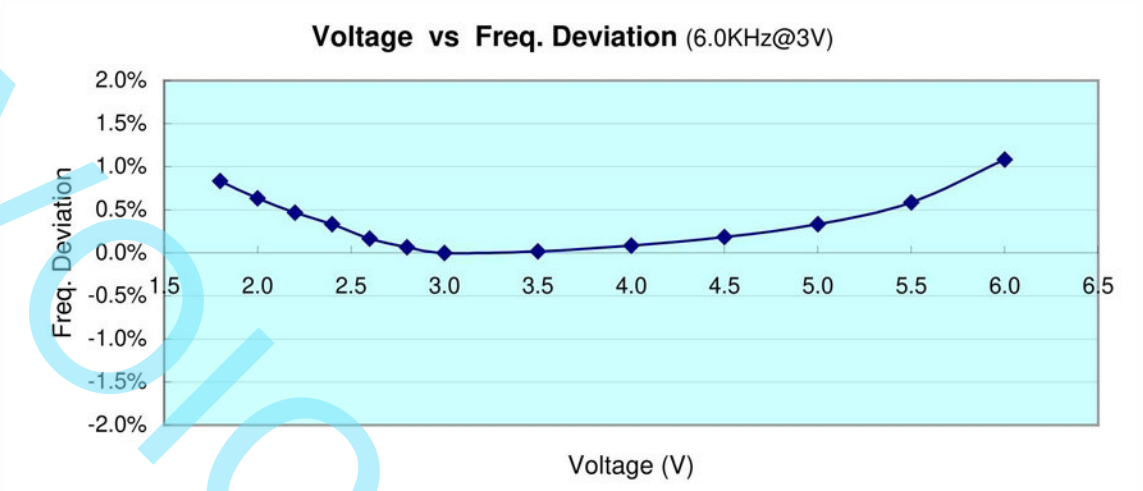
13.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
Vdd - Vss	Supply voltage	-0.5 ~ +6.0	V
Vin	Input voltage	Vss–0.3V ~ Vdd+0.3	V
Top	Operating Temperature	0 ~ +70	°C
Tst	Storage Temperature	-25 ~ +85	°C

13.2 DC Characteristics

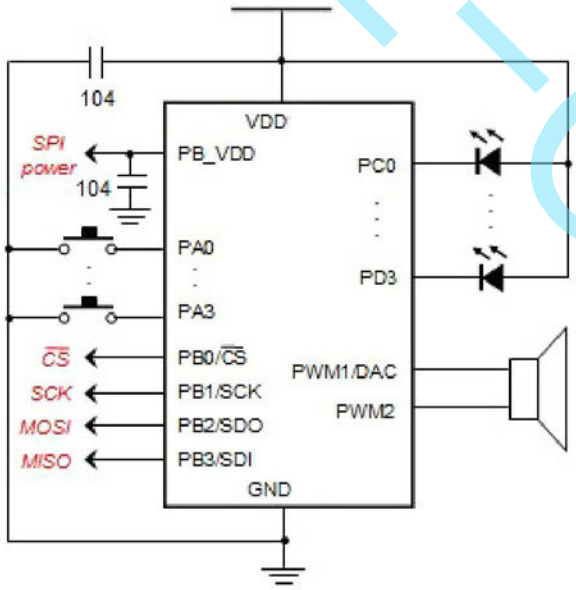
Symbol	Parameter		VDD	Min.	Typ.	Max.	Unit	Condition
VDD	Operating voltage			2.0	3	5.5	V	2MHz
I_{SB}	Supply current	Halt mode	3		0.1	0.5	uA	Sleep, no load
			4.5		0.1	0.5		
I_{SL}		Slow mode	3		55		uA	BT=16.384ms, no load
			4.5		70			
Iop		Operating mode	3		4.5		mA	2MHz, no loading
			4.5		5.5			
I_{IL}	Input current (Internal pull-high)	Weak (1.2M ohms)	3		2.5		uA	V_{IL}=0V
			4.5		7.4			
		Strong (120K ohms)	3		25		uA	
			4.5		70			
I_{OH}	Output high current		3		-7		mA	V_{OH}=2.0V
			4.5		-11			V_{OH}=3.5V
I_{OL}	Output low current (Normal current)	PA0	3		14		mA	V_{OL}=1.0V
			4.5		17			
		Other I/O	3		12		mA	
			4.5		17			
	Output low current (Large current)	PA0	3		28		mA	
			4.5		32			
		Other I/O	3		23		mA	
			4.5		32			
	Output low current (Constant current)		3		20		mA	
			4.5		21			
I_{PWM}	PWM output current (Normal)		3		60		mA	Load=8 ohms
			4.5		100			
	PWM output current (Ultra)		3		80		mA	
			4.5		125			
I_{DAC}	DAC output current		3		1.4		mA	Half scale
			4.5		1.6			
ΔF/F	Frequency deviation by voltage drop		3		-0.5		%	$\frac{Fosc(3.0v)-Fosc(2.4v)}{Fosc(3v)}$
			4.5		0.5			$\frac{Fosc(4.5v)-Fosc(3.0v)}{Fosc(4.5v)}$
ΔF/F	Frequency lot deviation		3	-0.5		0.5	%	$\frac{Fmax(3.0v)-Fmin(3.0v)}{Fmax(3.0v)}$
Fosc	Oscillation Frequency		-	1.90	2	2.05	MHz	VDD=2.0~5.5V

14.3 Voltage vs. Frequency

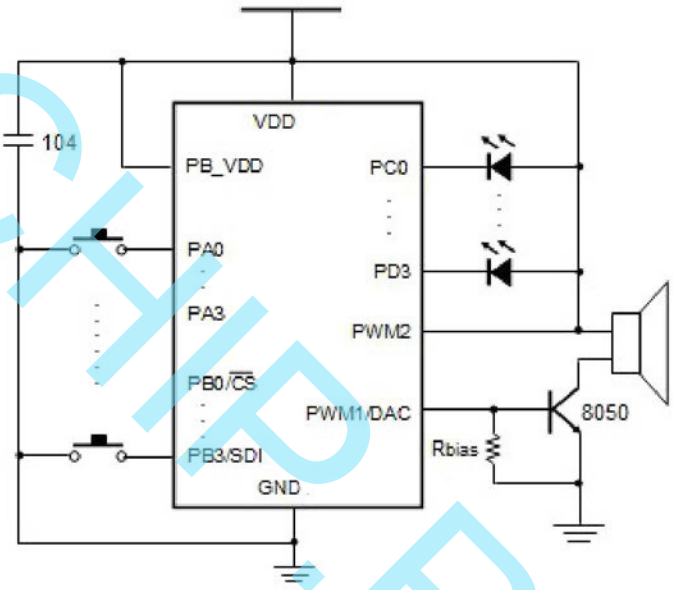


15. APPLICATION

(1) PWM Direct-Drive *(PB_VDD is set as LDO=3.3V)*



(2) DAC Output *(PB_VDD is set as floating)*



Note 1: If PB_VDD is set as LDO internally, PB_VDD pad is an output for the power of external SPI devices. And a 0.1uF capacitor is necessary to stabilize the LDO output voltage.

Note 2: If PB_VDD is set as floating internally, PB_VDD pad must be connected to VDD or external power supply.

16. PACKAGE